High-Resolution and Multi-Channel Time Interval Counter Using Time-to-Digital Converter and FPGA

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***Abstract*—A high-resolution and Multi-Channel time interval counter is designed using Time-to-Digital Converter(TDC) and(Field-Programmable-Gate-Array)FPGA. The core of counter is the TDC chip which is interfaced to and controlled by FPGA . The Counter has 1 start channel and 8 stop channels and can be provided with four different modes, and thus four different resolutions. In the highest resolution mode, the counter demonstrates a statistical standard deviation of 18.6 ps. In the lowest resolution mode, that is 82ps, the counter can work with 8 channels and be endless measurement range by internal retrigger of start. The measurement data can be read from the two FIFOs which are part of TDC as a form of real-time transfer or block. Therefore, the counter is communicated with personal computer by serial port RS232. This configuration provides an simply and efficient way of using a computer not only to control and operate the counter, but also to store and process measured data.**

I. INTRODUCTION

Precise time interval measurements are crucial in many areas of research and application, such as timekeeping systems, navigation positioning systems, laser distance measurement and so on. Specially, Multi-channel time interval counter are usually used in the GPS or other navigation positioning receiving system to compare several received time signals to a standard time reference signal[1]. In resent years, time digital converter (TDC) technology is widely developed and applied. The acquisition of physical dimensions can often be transformed into a measurement of time differences. In this paper, we structure a high-resolution and multi-channel time interval counter using TDC chip and Field-Programmable-Gate-Array(FPGA) technology. A personal computer (PC) software is used not only to control and operate the counter, but also to store and process measured data. Such design is easy and efficient and convenient to modify. The experimental results are presented and future work is discussed in the end.

II. DESIGN

Figure 1 depicts the proposed multi-channel time interval measurement architecture. There are 1 start input channel and 8 stop input channel which can accept TTL signals through BNC connector. In order to provide good impedance matching, 51k pull-down resistance is soldered in each input signal channels. The circuit is composed of three parts, a high-resolution and multi-channel TDC chip with 8-bit coarse counter, a FPGA block, a PC software. The TDC chip is the core of the time interval measurement. It includes high-resolution part and coarse counter part. The principle of high resolution of the TDC is based on digital tapped delay line within the phase-locked loop(PLL). The line is composed of a number of delay cells, i.e. logic gate unit, each having the same propagation delay. It can be picosecond resolution by modern CMOS technology. The use of the PLL ring oscillator can be regarded as a multiphase clock driving the clock inputs of the edge-triggered D-type flip-flops (DFFs) of the associated register, as shown in figure 2. Then the delay time can be precisely determined by counting the number of logic gate that start signal pass through. Because the logic gate propagation time depends upon voltage, temperature and the manufacturing process, the resolution of the TDC is not known and must be calculated via calibration measurements. In addition, the resolution is not stable with the swing of voltage and temperature. Therefore, the stable voltage supply and the resolution adjustment circuit is designed which uses voltage regulators. The PLL regulates the core voltage of the TDC so that the resolution is set exactly to the programmed value[2,3].

A 40MHz sine wave output from HP3335A synthesizer which is driven by the 10MHz rubidium clock signal is connected into a high speed comparator. The 40MHz TTL pulses from the comparator output with 3 ns rise time is fed to the reference clock input of the TDC chip. The jitter of the reference clock signal has direct effect on precise measurement when it is used as internal start retrigger signal, so the jitter is controlled below 80ps.

1-4244-0647-1/07/$20.00 ©2007 IEEE

The operation to the TDC is directly accomplished by FPGA module. First, FPGA implements the power-up reset, the registers configuration, enabling the measurement for TDC. Then the empty flags or the load-lever flags of the two interface FIFOs of TDC are checked. The former is helpful at low data and the latter is helpful at high data rate. As soon as the flag signal is activated, a single data or a block data can be read from the FIFOs. This depends on measurement mode and data rate. Thanks to the deep interface FIFO of the TDC, The interface with the computer becomes very simple using the RS232 controller in FPGA. The clocks in FPGA are synchronous with the main clock using a Digital Clock Manager(DCM). It ensures the credibility and stability of the whole design.

The PC software processes the measurement data when it receives the binary data from the serial RS232 interface. Then the measurement data are stored and displayed in the form of float. What is more, it sends the commands to FPGA which is regarded as a bridge between PC and TDC.

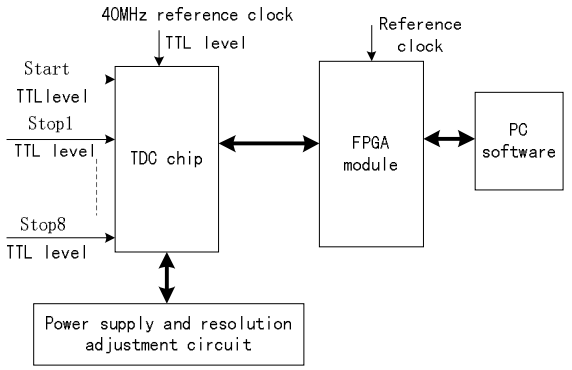

Figure 1. Block Diagram of the counter

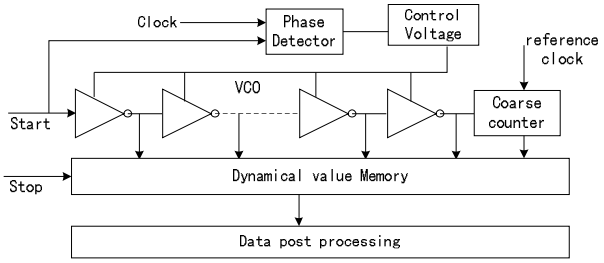

Figure 2. The principle diagram of TDC with the PLL

III. EXPERIMENTAL RESULTS

A self-test has been designed to verify the system precision. Figure 3 shows the block diagram of the self-test arrangement. The synthesized signal generator HP3335A which is synchronized with the rubidium frequency standard produces 40MHz sine wave signal to serve as the reference clock. The 1pps output from rubidium clock is divided into the two same signals through BNC divider. The two 1pps are connected to the start channel and stop1 or stop2 channel respectively and their time difference is about 12.6ns due to the fixed cable delay. The TDC is configured as the highest resolution mode. In this mode, the resolution is actually 10ps and the measurement range is from 0 ns to 40us and the quantization step showed in the figure 4 has no real influence. The TDC accepts only one stop event per channel, therefore the next measurement is made after Master-Reset or Partial-Reset.

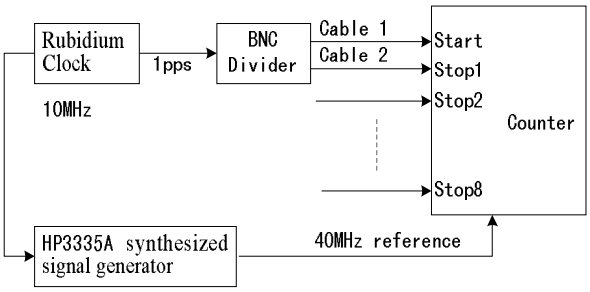

Figure 3. 1 pps Self-Test arrangement

Figure 4 is a time interval plot of a 65,000 s measurement run. The statistical results are showed. All of the readings are between the maximum 12.7159ns and the minimum 12.5787ns. The mean value is 12.6504ns and the standard deviation is 18.6ps.

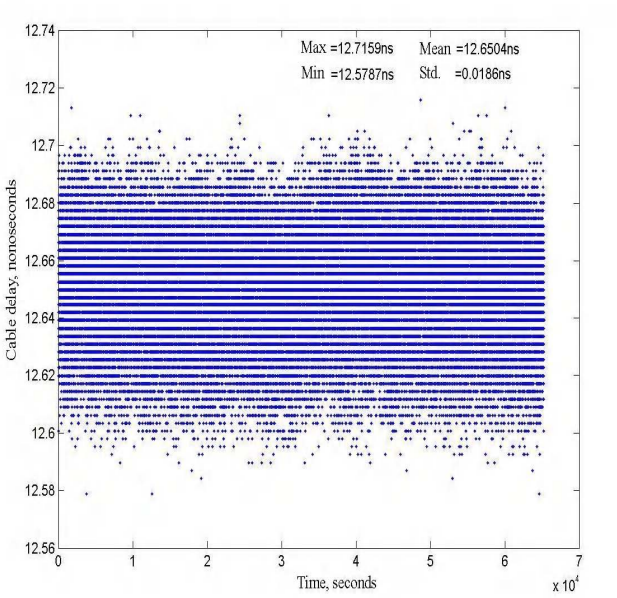

Figure 4. Self-test measurements data

In the multi-channel mode, the resolution of TDC is 82ps. There is an internal 8-bit counter which can take count of the start number. The start channel can only accept one initial start event. The period of the internal start repetition is programmable in multiples of the 40MHz reference clock and the internal counter is circular. Therefore, an unlimited measuring range can be made by internal start retrigger.Tabel1 lists the measurement data format of multi-channel. The block diagram of the multi-channel measurement arrangement is similar to figure 3. The 1kHz square wave signal is divided into the two same signals by BNC divider. The two 1kHz square wave signals which are connected into the channel1 and channel2 respectively and their time difference is about 12.6ns due to the fixed cable delay.

Table1 The format of multi-channel measurement data

Channel#	slope	Start#	measurement data
2	1	199	4814.813250 ns
2	1	66	2248.229722 ns
1	1	166	2248.476636 ns
2	1	166	2236.789397 ns
2	1	10	2248.476636 ns
1	1	110	2252.756470 ns
2	1	110	2240.986926 ns
2	1	210	2252.838774 ns
1	1	54	2253.332601 ns
2	1	54	2241.480753 ns
2	1	154	2250.781162 ns
1	1	254	2250.369639 ns
2	1	254	2238.435487 ns
1	1	198	2250.945771 ns
2	1	198	2239.423141 ns
2	1	42	2253.085687 ns
1	1	142	2252.838774 ns
2	1	142	2240.904621 ns
1	1	86	2251.604207 ns

Note: The slope "1" in the second column denotes positive slope.

IV. CONCLUSIONS AND FUTURE WORK

We have designed a high-precision and multi-channel time interval counter using TDC and FPGA. In the highest resolution mode, a standard deviation of self-test precision is 18.6ps. In the lowest resolution mode, when large range time interval measurements are involved like 1s, the measurement data are not intelligible enough due to the little coarse counter bit. We will improve the precision further and realize a FPGA multi-channel virtual time interval counter with a large measurement range about several decades seconds using the TDC chip in the future work.

[1] Andrew N. Novick, Michael A. Lombardi, Victor S. Zhang, "A High Performance Multi-Channel Time-Interval Counter With An Integrated GPS Receiver,"in Proc. 31st Precise Time and Time Interval Meeting(PTTI), 1999, pp.561-567.

[2] Arai Y and Ikeno M 1996 A time digitizer CMOS gate-array with a 250ps time resolution IEEE J. Solid State Circuits 31 212-20.

[3] J.Kalisz, 2004, "Review of methods for time interval measurements with picosecond resolution", Metrologia 41, 1-16.